C/ Formal Drawings
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: B. CHANDRAN ET AL.

Serial No.: 10/023,723

Filing Date: December 21, 2001

For: SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE PACKAGE-TO-DIE INTERCONNECT SCHEME FOR REDUCED DIE STRESSES

LETTER SUBMITTING FORMAL DRAWINGS

Assistant Commissioner for Patents
Washington, D.C. 20231

February 6, 2002

Sir:

Submitted herewith are three (3) sheets of formal drawings illustrating Figs. 1-10 in connection with the above-identified application.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

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